This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Original): A method for processing recess etch operations in substrates, comprising:

a) forming a hard mask over the substrate;

b) etching a trench in the substrate using the hard mask;

c) forming a dielectric layer over the hard mask and in the trench, the dielectric layer configured to line the trench;

d) applying a conductive material over the dielectric layer such that a blanket of the conductive material lies over the hard mask and fills the trench;

e) etching the conductive material to substantially planarize the conductive material, the etching of the conductive material being configured to trigger an end point just before all of the conductive material is removed from over the dielectric layer that overlies the hard mask; and

f) recess etching the conductive material so as to remove the conductive material over the dielectric layer that overlies the hard mask and removes at least part of the conductive material from within the trench.

Claim 2 (Original): A method for processing recess etch operations in substrates as recited in claim 1, further comprising:

repeating operations (c) through (f) one or more times to form multiple layers of the conductive material in the trench.

Claim 3 (Original): A method for processing recess etch operations in substrates as recited in claim 1, wherein the endpoint is triggered using interferometry monitoring.

Claim 4 (Original): A method for processing recess etch operations in substrates as recited in claim 3, wherein the hardmask is protected by utilizing the interferometry monitoring of the etching of the conductive material.

Claim 5 (Original): A method for processing recess etch operations in substrates as recited in claim 1, wherein the substantial planarization and the recess etching occurs in an etch chamber thereby increasing wafer production throughput.

Claim 6 (Original): A method for processing recess etch operations in substrates as recited in claim 1, wherein the etching of the conductive material utilizes a first chemistry including Cl_2, He, and SF_6.

Claim 7 (Original): A method for processing recess etch operations in substrates as recited in claim 6, wherein a Cl_2 flow rate is between about 20 sccms and about 200 sccms, a He flow rate is between about 20 sccms and about 500 sccms, and a SF_6 flow rate is between about 2 sccms and about 50 sccms.

Claim 8 (Original): A method for processing recess etch operations in substrates as recited in claim 1, wherein the recess etching utilizes a second chemistry including Ar and SF_6.

Claim 9 (Original): A method for processing recess etch operations in substrates as recited in claim 8, wherein an Ar flow rate is between about 0 sccms and about 300 sccms, and a SF_6 flow rate is between about 10 sccms and about 100 sccms.

Claim 10 (Original): A method for processing recess etch operations in substrates as recited in claim 1, wherein the recess etching is used with one of an interferometric endpoint (IEP) detection and a timed etching to monitor the removal of the conductive material.

Claim 11 (Original): A method for processing recess etch operations in substrates, comprising:

a) forming a hard mask over the substrate;

b) etching a trench in the substrate using the hard mask;

c) forming a dielectric layer over the hard mask and in the trench, the dielectric layer configured to line the trench;

d) applying a conductive material over the dielectric layer such that a blanket of the conductive material lies over the hard mask and fills the trench;

e) etching the conductive material using a first chemistry to substantially planarize the conductive material, the etching of the conductive material being configured to trigger an endpoint just before all of the conductive material is removed from over the dielectric layer that overlies the hard mask, the endpoint being triggered using interferometry monitoring;

f) recess etching the conductive material using a second chemistry and one of the interferometry monitoring and a timed etch so as to remove the conductive material over the

dielectric layer that overlies the hard mask and removes at least part of the conductive material from within the trench; and

g) repeating operations (c) through (f) one or more times to form multiple layers of the conductive material in the trench.

Claim 12 (Original): A method for processing recess etch operations in substrates as recited in claim 11, wherein the hardmask is protected by utilizing the interferometry monitoring of the etching of the conductive material.

Claim 13 (Original): A method for processing recess etch operations in substrates as recited in claim 11, wherein the substantial planarization and the recess etching occurs in an etch chamber thereby increasing wafer production throughput.

Claim 14 (Currently Amended): A method for processing recess etch operations in substrates as recited in claim 11, wherein the first chemistry ~~including~~ includes Cl_2, He, and SF_6.

Claim 15 (Original): A method for processing recess etch operations in substrates as recited in claim 14, wherein a Cl_2 flow rate is between about 20 sccms and about 200 sccms, a He flow rate is between about 20 sccms and about 500 sccms, and a SF_6 flow rate is between about 2 sccms and about 50 sccms.

Claim 16 (Currently Amended): A method for processing recess etch operations in substrates as recited in claim 11, wherein the second chemistry ~~including~~ includes Ar and SF_6.

Claim 17 (Original): A method for processing recess etch operations in substrates as recited in claim 16, wherein an Ar flow rate is between about 0 sccms and about 300 sccms, and a SF_6 flow rate is between about 10 sccms and about 100 sccms.

Claim 18 (Original): A method for processing recess etch operations in substrates, comprising:

a) forming a hard mask over the substrate;

b) etching a trench in the substrate using the hard mask;

c) forming a silicon dioxide layer over the hard mask and in the trench, the silicon dioxide layer configured to line the trench;

d) applying a polysilicon material over the dielectric layer such that a blanket of the polysilicon material lies over the hard mask and fills the trench;

e) etching the polysilicon material to substantially planarize the polysilicon material, the etching of the polysilicon material being configured to trigger an endpoint just before all of the polysilicon material is removed from over the silicon dioxide layer that overlies the hard mask, the endpoint is triggered using interferometry monitoring, the etching of the polysilicon material using a first chemistry including Cl_2, He, and SF_6; and

f) recess etching the polysilicon material using one of the interferometry monitoring and a timed etch so as to remove the polysilicon material over the silicon dioxide

layer that overlies the hard mask and removes at least part of the polysilicon material from within the trench, the recess etching using a second chemistry including Cl_2, He, and SF_6.

Claim 19 (Currently Amended): A method for processing recess etch operations in substrates as recited in claim 18, wherein a Cl_2 flow rate is about 100 sccms, a He flow rate is about 100 sccms, and a SF_6 flow rate is about 10 sccms.

Claim 20 (Original): A method for processing recess etch operations in substrates as recited in claim 19, wherein an Ar flow rate is about 200 sccms and a SF_6 flow rate is about 15 sccms.

Claim 21 (Currently Amended): A method for processing recess etch operations in substrates as recited in claim 18, wherein the planarization etching occurs in an etching chamber which utilizes a top power between 800 watts to about 1200 watts, a bottom power between 40 watts to about 100 watts, a gas pressure of between about 3 mTorr to about 10 mTorr, and a temperature of between about 10 degrees C and about 60 degrees C.

Claim 22 (Currently Amended): A method for processing recess etch operations in substrates as recited in claim 18, wherein the planarization etching occurs in an etching chamber which utilizes a top power of about 1000 watts, a bottom power of about 66 watts, a gas pressure of ~~about~~ about 5 mTorr, and a temperature of about 30 degrees C.

Claim 23 (Original): A method for processing recess etch operations in substrates as recited in claim 18, wherein the interferometry monitoring includes using a first light signal with a first wavelength, and a second light signal with a second wavelength, the first wavelength being different than the second wavelength.

Claim 24 (Original): A method for processing recess etch operations in substrates as recited in claim 18, further comprising:

repeating operations (c) through (f) one or more times to form multiple layers of the conductive material in the trench.